TDB-ACC-NO: NN72033176

DISCLOSURE TITLE: Self Aligning Metal to Polysilicon Contacts. March 1972.

PUBLICATION-DATA: IBM Technical Disclosure Bulletin, March 1972, US

VOLUME NUMBER: 14

ISSUE NUMBER: 10

PAGE NUMBER: 3176

PUBLICATION-DATE: March 1, 1972 (19720301)

CROSS REFERENCE: 0018-8689-14-10-3176

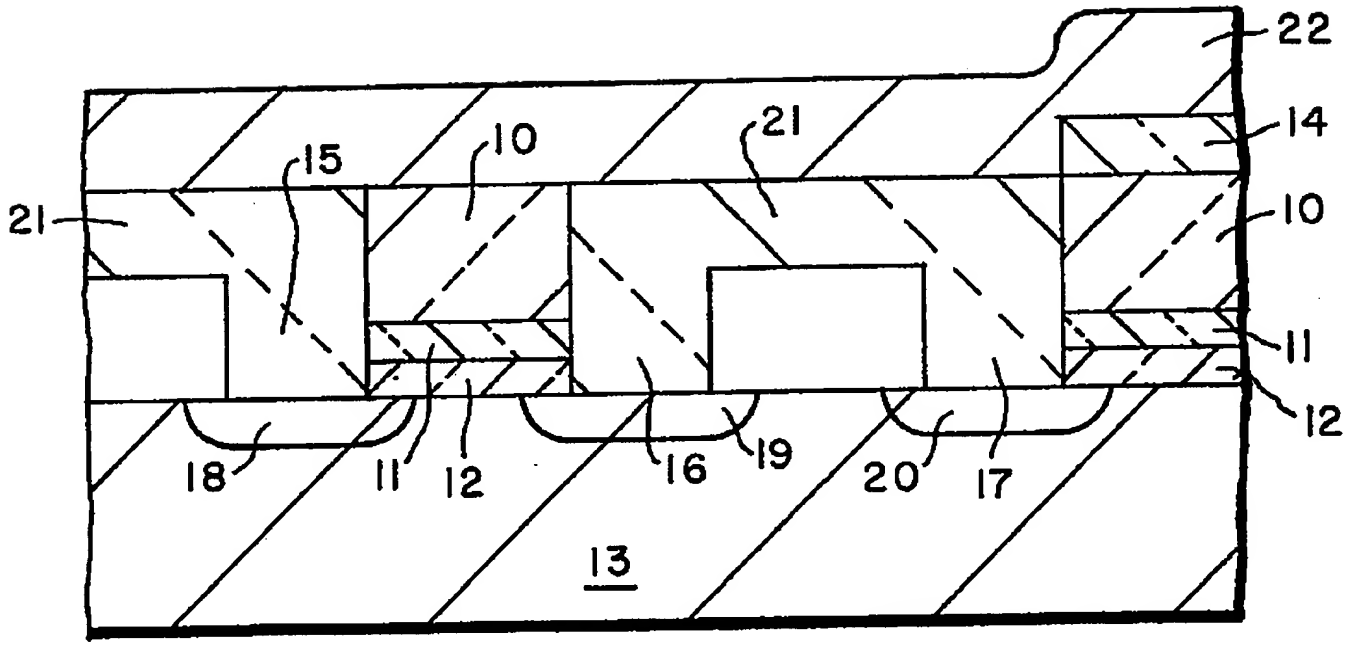
DISCLOSURE TEXT:

1p. The use of this process creates self-aligning polysilicon and metal contacts which are reduced approximately 75% from presently known and used modes of making such contact.

- In the so-called self-aligning gate process, a polysilicon layer 10 is laid down over layers of silicon nitride 11 and silicon dioxide 12 previously formed on the surface of a semiconductor body 13. The polysilicon layer 10 is then doped to reduce its resistivity and subsequently is covered with an insulator 14, such as titanium dioxide, which will not support the growth of thermal oxide but which will provide good insulation. The insulator 14 is then etched from selected regions and the underlying layers of polysilicon 10, silicon nitride 11 and silicon dioxide 12 are selectively etched to form diffusion windows 15, 16 and 17. The body 13 is then selectively diffused to form regions 18, 19 and 20 under windows 15, 16 and 17, respectively.

Simultaneously, with the drive in step following this diffusion of regions 18, 19 and 20, thick oxide layers 21 are formed over the diffused regions 18, 19 and 20. Contact holes are made to the diffused regions 18, 19 and 20 through this oxide layer 21, following which the insulator 14 is selectively removed from the surface of the polysilicon. Contact is then made to the polysilicon layer 10 by depositing metallic lines 22 over the device surface. It is to be noted that where contact between the polysilicon layer 10 and the metal line 22 is not desired the layer 14 is left intact.

- The polysilicon can be doped with appropriate impurities as it is being deposited.


22
14
21
15
10
21
10
11
12
18
11
12
16
19
20
17
13